SESSION 15 – TAPA III
Timing Generation

Friday, June 18, 1:30 p.m.
Chairpersons: G. Taylor, Intel
M. Nagata, Kobe University

15.1 — 1:30 p.m.
A 10+ GHz Low Jitter Wide Band PLL in 90 nm PD SOI CMOS Technology, D. Boerstler, K. Miki*, E. Hailu, H. Kihara**, E. Lukes***, J. Peter, S. Pettengill, J. Qi, J. Strom*** and M. Yoshida*, IBM Microelectronics, Austin, TX, *Toshiba America Electronic Components, **Sony Computer Entertainment of America, ***IBM Engineering and Technology Services, Rochester, MN

We report a wide band, low jitter PLL implemented in 90nm partially depleted (PD) Silicon-On-Insulator (SOI) CMOS technology. Using the thick and thin gate dielectric/oxide options available, two separate PLL designs are implemented. At a 1.5V supply, the maximum operating frequency of the PLL is 13.9 GHz and 7.5 GHz for the thin and thick gate oxide designs, respectively. At a 1.5V supply, with a feedback divide ratio of 8, cycle-to-cycle (C-C) jitter was measured at 14.2 ps P-P / 2.1 ps RMS and 11.1 ps P-P / 1.6 ps RMS for the thin and thick oxide designs, respectively. At 2.1V the maximum operating frequency of the thin oxide PLL is 17.3 GHz and at 16 GHz has 8.9 psP-P / 1.2 ps RMS C-C jitter, while the maximum frequency for the thick oxide PLL is 10.4 GHz. To our knowledge, these results show the highest frequency to date of any CMOS PLL and the lowest jitter of any known wide band CMOS PLL.

15.2 — 1:55 p.m.
A 0.6-1.2V, Low-Power Configurable PLL Architecture for 6GHz-300MHz Applications in a 90nm CMOS Process, P. Raha, Texas Instruments, Inc., Dallas, TX

This paper presents a configurable feed-forward PLL architecture with supply-independent loop for dynamics for low power, multiphase clock-generation in power-sensitive DSP cores using dynamic voltage scaling techniques in a 90nm CMOS process. A four-stage, current-controlled ring-oscillator based PLL is shown to be able to generate 6GHz-300MHz frequencies in a 90nm CMOS process with a power supply range of 1.2-0.6V. PLL power consumption is 10mW@5GHz and 300uW@500MHz. The PLL die area is 0.10mm2.

15.3 — 2:20 p.m.
A Background Optimization Method for PLL by Measuring Phase Jitter Performance, S. Dosho and N. Yanagisawa, Matsushita Electric Industrial Co., Ltd., Osaka, Japan

This paper describes a background(BG) optimization method for Phase-Locked-Loop(PLL). Measuring the phase shift of the voltage controlled oscillator(VCO) at each input reference clock, we can determine the phasejitter performance exactly. Using the combination of the global optimization method at initial phase and the local optimization method for background calibration always gives the PLL the smallest jitter performance under any conditions.

15.4 — 2:45 p.m.
A Sampling Oscilloscope Macro Toward Feedback Physical Design Methodology, M. Takamiya and M. Mizuno, NEC Corporation, Kanagawa, Japan

The sampling oscilloscope macro fabricated with a 1.0 V 90-nm CMOS process occupies 350 um x 140 um and achieves 68%-increase of the operation frequency and the input voltage range of 2 V. The macro is easy to be embedded in an actually operating LSI, because it requires no dedi-cated power supply, no analog I/O, and no dedicated clock signal. By using the macro, the world's first measurement of an undershooting waveform caused by an on-chip inductive effect has demonstrated at 2.2-GHz clock.

Break 3:10 p.m.